UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,073	10/19/2000	Coke Reed	F.11146	6301

7590 04/04/2005

KEITH D. NOWAK
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 AVENUE OF THE AMERICAS
41ST FLOOR
NEWYORK, NY 10036-2714

EXAMINER	
KADING, JOSHUA A	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,073	REED ET AL.	
	Examiner	Art Unit	
	Joshua Kading	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9 and 11-18* is/are rejected.

7)☒ Claim(s) *4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

The claims are objected to because they include reference characters which are not enclosed within parentheses.

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

Regarding claims 1-9, 11-14, and 16-18, applicant has asked for an example of the characters in the claims that have caused the objection. For example, claim 1, line 2 states, "nodes A and E". The "A" and "E" must be in parentheses because the "nodes A and E" are disclosed in the specification at page 7, line 22. Further, claims 3 and 4 disclose, "control signal z" and "control signal y...control signal x" respectively. The letters "x", "y", and "z" should be in parentheses as well for similar reasons as with the nodes A and E. Finally, there are instances of "a message MB" or "a message MA" such as in claim 9. These too should be in parentheses for the same reasons as stated above. It should also be noted that the above are examples of instances in the claims where characters should be placed in parentheses. However, these examples are not meant to be exhaustive of all characters in the claims that need to be placed in parentheses. Other characters not mentioned that are required to be placed in parentheses should be.

Claims 16-18 are objected to because of the following informalities:

Regarding claims 16-18, each discloses, messages "M_A" and "M_B". However, other claims, including dependent claims 11, 12, and 18 disclose messages "MA" and "MB". It is not clear if, for instance, "MA" and "M_A" refer to the same message. Therefore, these should be changed to be consistent with the rest of the claim language. Applicant is reminded that these messages "MA" and "MB" should also be put in parentheses in accordance with MPEP § 608.01(m).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11, 12, and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claim 16 (parent claim of claims 11 and 12), applicant discloses, "all output ports accessible from I_A being accessible from output O_D." It is unclear from the specification how this is possible. For instance, figures 6B and 6C show node C with all of its output ports and all the output ports of nodes D and H

accessible from the input port coming from node A (i.e. input port I_A). However, the output ports of node H will never be accessible from the output port of node C going to node D (i.e. output port O_D will never connect to node H and thus cannot have access to the output ports of node H). How then, can "all output ports accessible from I_A [be] accessible from output O_D," when the figures seem to contradict this limitation?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 17, the last limitation of claim 17 states, "...there is a path through output port O_D to a target destination for message M_B and a path through output port O_H to a target destination for message M_B." Are both outputs supposed to output message M_B and if so, what happens to message M_A?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,272,141 B1, Reed.

Regarding claim 1, Reed discloses "an interconnect structure, comprising:

a plurality of interconnected nodes, including distinct nodes A and E (figure 3A, element 324 acts as applicant's node A, element 332 acts as applicant's node E);

a routing logic associated with the nodes (col. 20, lines 24-28 where this is describing a generic node setup), the routing logic for routing data selectively among the interconnected nodes (col. 8, lines 52-55);

the nodes A and E being positioned in the interconnect structure so that node A cannot route data to the node E, the node E cannot route data to the node A (figure 3A, where it is clear from the data path lines that element 324 cannot route data to element 332 and vice versa), and no node exists in the interconnect structure that can have data routed directly to it from both the node A and the node E (figure 3A, where it is again clear that no node can have data sent to it directly from elements 324 or 332); and

a logic included as part of said routing logic and associated with the node A that uses information concerning routing of data through the node E to route data through the node A (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 324 and 332 to communicate this control information with each other as well)."

However, Reed explicitly lacks nodes A and E having "the node A having a plurality of data input ports, a plurality of data output ports, a control signal output port;

and the node E having a plurality of data input ports, a plurality of data output ports, a control signal output port."

Although Reed does not explicitly disclose the plurality of input ports, plurality of output ports, and control signals in each node in figure 3A, figure 2 elements 210 and 212 show the input ports, elements 220 and 222 show the output ports, and element 224 shows a control output, thus it is reasonable to assume that each node of figure 3A will have a plurality of input ports, plurality of output ports, and a control output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time of invention to include the plurality of input and output ports and control signal output port with the nodes for the purpose of sending control information about message transmissions to other nodes in the interconnect. The motivation for sending control information to other nodes about message data is so that each node receives only one message at a time and thus preventing data contention (Reed, col. 8, lines 63-65).

Regarding claim 2, Reed discloses "an interconnect structure in accordance with claim 1 wherein: the plurality of interconnected nodes includes a node F distinct from the nodes A and E (figure 3A, element 330 is node F), the node F...a control signal output port (figure 3A, the dashed line coming out of element 330 represents a control signal coming from a control signal port); and the nodes A and F are positioned in the interconnect structure so that the node A cannot route data to the node F, the node F cannot route data through the node A (figure 3A, where it is clear that elements 324 and

330 cannot route data to one another), and no node exists in the interconnect structure that can receive data directly routed both from the node A and the node F (figure 3A, where it is again clear that no node can receive data directly from both elements 324 and 330); and the logic associated with the node A uses information concerning routing of data through the node F to route data through the node A (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 324 and 330 to communicate this control information with each other as well)."

However, Reed explicitly lacks node F "...having a plurality of data input ports, a plurality of data output ports..." As with claim 1, Reed does disclose in figure 2 elements 210 and 212 that show the input ports and elements 220 and 222 that show the output ports, thus it is reasonable to assume that each node of figure 3A will have a plurality of input ports and plurality of output ports even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time of invention to include the plurality of ports with the interconnect of claim 1 for the same reasons and motivation as in claim 1.

Regarding claim 3, Reed discloses "an interconnect structure in accordance with claim 2 wherein: the plurality of interconnected nodes includes a node B distinct from the nodes A, E and F (figure 3A, element 322 acts as applicant's node B); and a logic associated with node B included as part of the routing logic (col. 20, lines 24-28 where this is describing a generic node setup)... the control signal z containing information

concerning routing possibilities through the nodes B, F and E, and the logic associated with the node A for routing of data through the node A depending at least in part on information concerning routing of data through the nodes B, F and E (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 322, 330, 324, and 332 to communicate this control information with each other as well)."

However, Reed explicitly lacks "the node B having a plurality of data input ports, a plurality of data output ports, and a control signal output port... being capable of sending a control signal z to the node A..."

As with previous claims, Reed does disclose in figure 2 elements 210 and 212 that show the input ports, elements 220 and 222 that show the output ports, and element 224 that shows a control output, thus it is reasonable to assume that each node of figure 3A will have a plurality of input ports, plurality of output ports, and a control output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time of invention to include the plurality of ports with the interconnect of claim 1 for the same reasons and motivation as in claim 1.

Regarding claim 5, Reed discloses "an interconnect structure comprising:

a plurality of nodes including distinct nodes A, B and C, the nodes A and B being both positioned to send data to the node C (figure 3A, element 324 acts as applicant's

node A, element 322 acts as applicant's node B, and element 320 acts as applicant's node C);

a plurality of interconnect lines selectively coupling the nodes of the interconnect structure (figure 3A, all the data paths between the nodes);

a routing logic associated with the node B capable of sending data to the node C and sending a control signal to the node A that can inform the node A that the node A is allowed to send a message to the node C (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 320 and 332 to communicate this control information with each other as well)."

However, Reed explicitly lacks "a control signal carrying line connected from the node B to the node A for carrying control signals from the node B to the node A..."

Although Reed does not explicitly disclose the control signal in each node in figure 3A, figure 2 element 224 shows a control output for a generic type node, thus it is reasonable to assume that each node of figure 3A will have a control output even if it is not explicitly drawn.

It would have been obvious to one with ordinary skill in the art at the time of invention to include the control signal output port with the nodes for the purpose of sending control information about message transmissions to other nodes in the interconnect. The motivation for sending control information to other nodes about message data is so that each node receives only one message at a time and thus preventing data contention (Reed, col. 8, lines 63-65).

Regarding claim 6, Reed discloses the interconnect of claim 5 and "the node C has a plurality of input ports (figure 3A, element 320 has a plurality of inputs from other nodes)..."

However, Reed explicitly lacks "...data from the nodes A and B arrive at the node C concurrently so that all of the input ports of the node C receive messages simultaneously." Although Reed does not explicitly state that the data arrives simultaneously, it can be reasonably assumed from figure 3A that node C (element 320) can receive data from element 324 and element 322 as the inputs from each node are independent of one another and thus data sent from either or both nodes can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time of invention to have the inputs of node C receive data simultaneously with the interconnect of claim 5 for the same reasons and motivation as in claim 5.

Regarding claim 7, Reed discloses the interconnect of claim 6 and "the plurality of nodes includes distinct nodes A, B, C, D, E, F and H (figure 3A, element 324 acts as node A, element 322 acts as node B, element 320 acts as node C, element 332 acts as node E, element 330 acts as node F, element 326 acts as node D, and element 328 acts as node H)..."

However, Reed explicitly lacks "the node C is capable of simultaneously sending data from the node A to the node D, and capable of sending data form the node B to the node H."

Although Reed does not explicitly state that the data arrives simultaneously, it can be reasonably assumed from figure 3A that node C (element 320) can transmit data to element 326 and element 328 as the outputs from node C are independent of one another and thus data sent to either or both nodes D and E can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time of invention to have the outputs of node C send data simultaneously with the interconnect of claim 5 for the same reasons and motivation as in claim 5.

Regarding claim 9, Reed discloses "an interconnect structure comprising:

a plurality of nodes...including the distinct nodes A, B and C, and a collection of interconnect lines selectively coupling the nodes (figure 3A, element 324 acts as node A, element 322 acts as node B, and element 320 acts as node C);

the node C having a plurality of message input ports, the nodes A and C positioned in the structure so that A can route a data packet to C (figure 3A where element 320 has a plurality of inputs and can receive data from element 324);

the nodes B and C positioned in the structure so that B can route a data packet to C (figure 3A where element 320 can receive packets from element 322)...

logic at the node A using the control signal from node B to route messages (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 324 and 332 to communicate this control information with each other as well)..."

However, Reed explicitly lacks each node "adapted to generate a control signal" and "the nodes A and B positioned in the network so that B can send a control signal to A; the node B routing a message MB to C; the node A routing a message MA to C to arrive at concurrently with MB; all input ports of C concurrently receiving a message."

Although Reed does not explicitly disclose the control signal in each node in figure 3A, figure 2 element 224 shows a control output for a generic type node, thus it is reasonable to assume that each node of figure 3A will have a control output even if it is not explicitly drawn.

Further, it is implied by the data paths drawn between the nodes that messages can be sent from one node to another, and although Reed does not explicitly state that the data arrives concurrently at node C, it can be reasonably assumed from figure 3A that node C (element 320) can receive data from element 324 and element 322 as the inputs of node C are independent of one another and thus data sent to either or both inputs can arrive simultaneously.

It would have been obvious to one with ordinary skill in the art at the time of invention to include the control signal output port with the nodes for the purpose of sending control information about message transmissions to other nodes in the interconnect. The motivation for sending control information to other nodes about message data is so that each node receives only one message at a time and thus preventing data contention (Reed, col. 8, lines 63-65).

Claims 13-15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed in view of U.S. Patent 5,940,389, Yang et al. (Yang).

Regarding claim 13, Reed discloses "an interconnect structure comprising:

a plurality of interconnected nodes including nodes A, B, C, D, and H (figure 3A, element 324 acts as node A, element 322 acts as node B, element 320 acts as node C, element 326 acts as node D, and element 328 acts as node H), each of the nodes A, B, C, D and H having a plurality of input ports and a plurality of output ports (figure 2 elements 210 and 212 show the input ports and elements 220 and 222 show the output ports of a generic node in the interconnect), and node C being positioned to receive messages from A and B and to route messages to D and H (figure 3A shows element 320 being positioned to receive data from elements 324 and 322 and send data to elements 326 and 328);

a plurality of interconnect structure output ports including an output port that is accessible from node C but not node H (figure 3A where as seen there are a plurality of output ports on each node and there is an output port from element 320 to element 326 that is clearly not accessible from element 328);

a routing logic included within the interconnect structure (col. 20, lines 24-28 where this is describing a generic node setup)..."

However, Reed lacks what Yang discloses, the routing logic is "to assure that when node A sends a message MA to node C and concurrently node B sends a message MB to node C, then node C can route MA through node D to a target

interconnect structure output port for MA and node C can route MB through node H to a target interconnect structure output port for MB (figure 10, where the first node of stage 0 can receive input from two ports, like element 320 of Reed, and as indicated by the data paths drawn can send concurrent messages to two different nodes, such as elements 326 and 328 of Reed)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the assurance of messages being routed from an input to an output for the purpose of creating a non-blocking set of nodes (Yang, col. 7, lines 3-31). The motivation for having a non-blocking set of nodes is the advantage of having a plurality of data being transported through the nodes without any being lost or blocked because of contention issues.

Regarding claim 14, Reed and Yang disclose the interconnect of claim 13. However, Reed lacks what Yang further discloses, "said routing logic assures that message MB is not blocked from node H, and message MA is not blocked from node D (col. 7, lines 3-31 where by the very nature of the node setup, the outputs are not blocked)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the non-blocking with the interconnect of claim 13 for the same reasons and motivation as in claim 13.

Regarding claim 15, Reed and Yang disclose the interconnect claim 14. However, Reed lacks what Yang further discloses, "said routing logic for the routing of

messages MA and MB depends in part on QOS criteria (col. 21, lines 26-31 as is known in the art, priority of data is a QoS criteria)." It would have been obvious to one of ordinary skill in the art at the time of invention to include the QoS criteria with the interconnect of claim 14 for the same reasons and motivation as in claim 14.

It will be assumed that the message M_B through input port I_B and output port O_D is actually supposed to be message M_A.

Regarding claim 17, Reed discloses, "an interconnect structure comprising: a plurality of interconnected nodes including a node C having input ports I_A and I_B and output ports O_H and O_D (figure 3A, element 320 represents "node C" where there are two inputs I_A and I_B from top to bottom and two outputs O_H and O_D from top to bottom); a plurality of output ports that are accessible from input port I_B but not from output O_H (figure 3A, element 328 where although there are no outputs shown for element 328, it can be reasonably assumed the node has outputs and thus these outputs are only accessible from output port O_D)..."

However, Reed lacks what Yang discloses, "a routing logic included within the interconnect structure to assure that when a message M_A arrives at input port I_A and simultaneously a message M_B arrives at input port I_B there is a path through output port O_D to a target destination for message M_A and a path through output port O_H to a target destination for message M_B (figure 10, where the first node of stage 0 can receive input from two ports, like element 320 of Reed, and as indicated by the data paths drawn can

send concurrent messages to two different nodes, such as elements 326 and 328 of Reed)."

It would have been obvious to one with ordinary skill in the art at the time of invention to include the assurance of messages being routed from an input to an output for the purpose of creating a non-blocking set of nodes (Yang, col. 7, lines 3-31). The motivation for having a non-blocking set of nodes is the advantage of having a plurality of data being transported through the nodes without any being lost or blocked because of contention issues.

Regarding claim 18, Reed and Yang disclose the interconnect of claim 17. However, Reed lacks what Yang further discloses, "said routing logic assumes that message MB is not blocked from using the first output port and message MA is not blocked from using the second output port (col. 7, lines 3-31 where by the very nature of the node setup, the outputs are not blocked)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the non-blocking with the interconnect of claim 17 for the same reasons and motivation as in claim 17.

Allowable Subject Matter

Claims 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments, see REMARKS, page 10, paragraph 3, filed 21 October 2004, with respect to the objections of claims 9 and 13 have been fully considered and are persuasive. The objections of claims 9 and 13 have been withdrawn.

Applicant's arguments, see REMARKS, page 11, paragraph 1, filed 21 October 2004, with respect to the 35 U.S.C. 112, first paragraph rejection of claim 8 have been fully considered and are persuasive. The 35 U.S.C. 112, first paragraph rejection of claim 8 has been withdrawn.

Applicant's arguments filed 21 October 2004 have been fully considered but they are not persuasive.

Regarding the rejection of claims 1-3, 5-7, and 9 applicant argues that Reed fails to disclose applicant's invention because Reed does not disclose each node with a plurality of inputs, outputs, and control signals. The examiner respectfully disagrees.

Although the particular figure used in Reed to reject applicant's claimed invention does not explicitly show a plurality of input ports, output ports, and control lines on each node (as admitted in the Office Action), figure 2 of Reed does disclose a node (as described in col. 6, lines 63-64) with a plurality of inputs (210 and 212), outputs (220 and 222), and control lines (214 and 224). It would have been obvious to one of ordinary skill in the art at the time of invention to impart the features of the node of figure 2 on all other nodes in Reed's invention. The reason being that there is no mention in

Reed that this is not possible or that the nodes of figure 3A are somehow different than the node pictured in figure 2. Just because a figure does not show all possible elements of a node does not mean they don't exist or that it would not have been an obvious expedient to include them. In this case, figure 2 provides the justification for one of ordinary skill in the art to assume a plurality of input lines, output lines, and control lines to any node of Reed.

Regarding the rejection of claims 10-15 applicant argues that the nodes of Yang are not "genuine switching nodes" and that Yang does not read on the invention because "the node is [not] always set in the bar position." The examiner respectfully disagrees.

First, what is a "genuine switching node?" Applicant seems to assume that a "genuine switching node" is one with two inputs and two outputs that allow messages received at any input to be switched to either output (REMARKS, page 12, lines 21-22). What then is a node with 3 (or more) inputs and 3 (or more) outputs that performs the same function? However, assuming that applicant's switches are genuine, Yang does in fact also disclose "genuine switching nodes." As seen in figure 10 each stage has 4 nodes, each with two inputs and two outputs capable of switching a message from any input node to any output node. The particular configuration of Yang in figure 10 is merely one of many configurations of the switch. This is supported in col. 7, lines 3-8 and 12-13. Therefore, Yang's switch fully reads on applicant's claimed invention.

Lastly, applicant seems to argue that the claimed invention is of a switch in a "bar position." However, this seems to conflict with what applicant argues previously about

the switch being "genuine". Further, no part of any claim discloses a switch in a bar position. But for the sake of argument assuming applicant's switch is in the bar position, Yang still reads on applicant's invention because Yang fully discloses a switch that can operate in a bar position. Applicant even admits this in the REMARKS, page 13, lines 11-14.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (571) 272-3070. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joshua Kading
Examiner
Art Unit 2661

March 24, 2005

BOB PHUNKULH
PRIMARY EXAMINER